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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/594,561	09/27/2006	Kazumasa Tanida	AI-427NP	5593

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RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
ARROYO, TERESA M	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
10/05/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,561	TANIDA ET AL.	
	Examiner	Art Unit	
	TERESA M. ARROYO	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-102* is/are pending in the application.

4a) Of the above claim(s) *38-102* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-23,25-31 and 33-37* is/are rejected.

7)☒ Claim(s) *24 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/18/09* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 16-37 in the reply filed on 06/29/11 is acknowledged.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the functional surface is formed not entirely on one surface of the semiconductor chip (claim 32) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 32 objected to because of the following informalities: The terminology the functional surface is formed not entirely on one surface of the semiconductor chip is not understood because there is no description of such a feature in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 16-23, 25, 31, 37 rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Pub. No. 2002/0043704 to Seko.

Regarding claim 16, Seko discloses A semiconductor device, comprising:

a solid state device 11 having a surface (top) and an external connection surface (bottom) which is a surface on a side opposite the surface (top),

a semiconductor chip 14 having a functional surface (bottom),

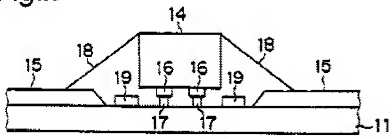
a connecting member 16 provided between the surface (top) of the solid state device 11 and the functional surface (bottom) of the semiconductor chip 14, the connecting member 16 extending over a distance between the surface (top) of the solid

state device 11 and the functional surface (bottom) of the semiconductor chip 14 and having a constant width,

an insulating film 15 provided on the surface (top) of the solid state device 11, the insulating film 15 having an opening (unlabeled) greater in size than the semiconductor chip 14, and

a sealing layer 18 that completely seals the opening (unlabeled) and a space between (unlabeled) the solid state device 11 and the semiconductor chip 14.

Fig.2



Regarding claim 17, Seko discloses The semiconductor device according to claim 16, wherein a connection pad 17 is provided on the surface (top) of the solid state device 11.

Regarding claim 18, Seko discloses The semiconductor device according to claim 17, wherein the connecting member 16 includes the connection pad 17.

Regarding claim 19, Seko discloses The semiconductor device according to claim 17, wherein the solid state device 11 and the semiconductor chip 14 are bonded by means of the connecting member 16 including the connection pad 17 with a predetermined interval between the solid state device 11 and the semiconductor chip 14.

Regarding claim 20, Seko discloses The semiconductor device according to claim 16, wherein the solid state device 11 and the semiconductor chip 14 are electrically connected together.

Regarding claim 21, Seko discloses The semiconductor device according to claim 16, wherein the insulating film 15 is a solder resist film.

Regarding claim 22, Seko discloses The semiconductor device according to claim 16, wherein the insulating film 15 has a thickness smaller than an interval between the surface of the solid state device 11 and the semiconductor chip 14.

Regarding claim 23, Seko discloses The semiconductor device according to claim 16, wherein the opening (unlabeled) of the insulating film 15 is formed so that the semiconductor chip 14 completely falls laterally within the opening (unlabeled).

Regarding claim 25, Seko discloses The semiconductor device according to claim 16, wherein the sealing layer 18 is provided in such a manner as to fill the opening (unlabeled) with the sealing layer 18, and wherein the sealing layer 18 [serves to] seal a gap between the solid state device 11 and the semiconductor chip 14 and [to] protect the functional surface (bottom), the connecting member 16 and an exposed part of the surface (top) of the solid state device 11 exposed from the opening (unlabeled) of the insulating film 15. Note the terminology in brackets is functional language not being given any patentable weight.

Regarding claim 31, Seko discloses The semiconductor device according to claim 16, wherein the semiconductor chip 11 has the functional surface (bottom) only on one surface of the semiconductor chip 11.

Regarding claim 37, Seko discloses The semiconductor device according to claim 16, wherein no other wiring than a connection pad 17 for connection with the semiconductor chip 14 is provided on the solid state device 11 in the opening (unlabeled) of the insulating film 15.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

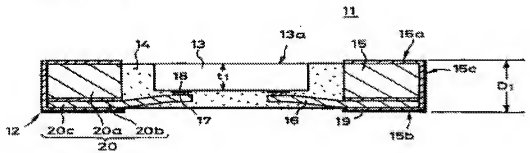
consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 26-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Seko as applied to claim 16 above, and further in view of US Patent No. 5723900 to Kojima et al.

Regarding claim 26, Seko fails to disclose The semiconductor device according to claim 16, wherein an end electrode that is electrically connected to the connecting member is formed at an end of the solid state device.

Kojima et al. teach a semiconductor device including an end electrode 15c connected to a connecting member 18 formed at an end of a solid state device 15.

FIG. 2



Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an end electrode in Seko since they are well-known in the art to mount a package from any surface as taught by Kojima et al. in col. 5, lines 36-43.

Regarding claim 27, Kojima et al. teach The semiconductor device according to claim 26, wherein the end electrode 15c leads from the surface (top) to the external connection surface (bottom) via an end face on the solid state device 15.

Regarding claim 28, Kojima et al. teach The semiconductor device according to claim 26, wherein the semiconductor device 13 [can] establish an electric connection with other wiring board 29 (Fig. 6) in the end electrode 15c. Note terminology in brackets is indefinite as to whether the features following it are intended to be part of the claim.

8. Claim 29, 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Seko as applied to claim 16 above, and further in view of US Patent No. 6515370 to Hashimoto.

Regarding claim 29, Seko fails to disclose The semiconductor device according to claim 16, wherein the semiconductor chip includes two [or more] semiconductor chips each connected to the solid state device in a flip chip manner. Note terminology in brackets should be changed to at least two for clarity.

Hashimoto teaches a semiconductor device including two or more semiconductor chips 54 connected to a solid state device 58 in a flip chip manner.

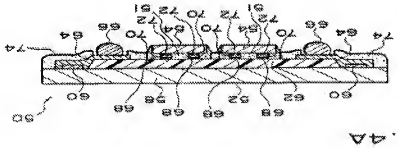


FIG. 4A

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a plurality of chips in Seko since mere duplication of parts of an invention is of no patentable weight unless a new and useful

product results and since Hashimoto teaches two or more chips for a multi0chip module on a solid state device in col. 7, line 52 to col. 8, line 4.

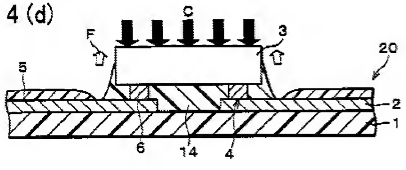
Regarding claim 30, Hashimoto teaches The semiconductor device according to claim 29, wherein the opening (unlabeled) of the insulating film 74 includes two or more openings (openings) each completely laterally including each semiconductor chip 54.

9. Claim 33-36 rejected under 35 U.S.C. 103(a) as being unpatentable over Seko ('704) as applied to claim 16 above, and further in view of US Patent Pub. No. 2004/0061240 to Seko ('240).

Regarding claim 33, Seko ('704) fails to disclose The semiconductor device according to claim 16, wherein the sealing layer is not on the insulating film.

Seko teaches a semiconductor device including a sealing layer 14 not on an insulating film 5.

FIG. 4 (d)



Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide a sealing layer not on an insulating film in Seko ('704) based on routine engineering design considerations as shown in Seko ('240).

Regarding claim 34, Seko ('240) teachesThe semiconductor device according to claim 16, wherein the sealing layer 14 at least partially covers a side surface of the semiconductor chip 3.

Regarding claim 35, Seko ('240) teaches The semiconductor device according to claim 34, wherein the sealing layer 14 does not reach an upper surface of the semiconductor chip 3.

Regarding claim 36, Seko ('240) teaches The semiconductor device according to claim 35, wherein the sealing layer 14 is not on the insulating film 5.

Allowable Subject Matter

10. Claim 24 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: None of the cited prior art discloses or teaches wherein a lateral distance between an outer periphery of the semiconductor chip and an edge of the opening of the insulating film is 0.1 mm or more.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The other cited prior art on PTO-892 teaches a solder resist on a solid state device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TERESA M. ARROYO whose telephone number is

(571)272-7260. The examiner can normally be reached on M-F, varying hours 5:30 AM-10:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571) 272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TERESA M ARROYO/
Examiner, Art Unit 2826